**GENERAL DESCRIPTION**

The HI-8599 from Holt Integrated Circuits is a silicon gate CMOS device for interfacing a 16-bit parallel data bus directly to the ARINC 429 serial bus. This device provides two receivers, an independent transmitter and line driver capability in a single package. The receiver input circuitry and logic are designed to meet the ARINC 429 specifications for loading, level detection, timing, and protocol. The transmitter section provides the ARINC 429 communication protocol and the line driver circuits provide the ARINC 429 output levels.

The 16-bit parallel data bus exchanges the 32-bit ARINC data word in two steps when either loading the transmitter or interrogating the receivers. The data bus interfaces with CMOS and TTL.

The HI-8599 provides the option to bypass most of the internal output resistance so that external series resistance may be added for lighting protection and still match the 75 ohm characteristic impedance of the ARINC bus.

Each independent receiver monitors the data stream with a sampling rate 10 times the data rate. The sampling rate is software selectable at either 1MHz or 125KHz. The results of a parity check are available as the 32nd ARINC bit. The HI-8599 examines the null and data timings and will reject erroneous patterns. For example, with a 125 KHz clock selection, the data frequency must be between 10.4 KHz and 15.6 KHz.

The transmitter has a First In, First Out (FIFO) memory to store 8 ARINC words for transmission. The data rate of the transmitter is software selectable by dividing the master clock, CLK, by either 10 or 80. The master clock is used to set the timing of the ARINC transmission within the required resolution.

The HI-8599 is nearly identical to the HI-8589 but has a TEST input pin not found in the HI-8589.

**APPLICATIONS**

- Avionics data communication
- Serial to parallel conversion
- Parallel to serial conversion

**FEATURES**

- ARINC specification 429 compliant
- Direct receiver and transmitter interface to ARINC bus in a single device
- 16-Bit parallel data bus
- Timing control 10 times the data rate
- Selectable data clocks
- Receiver error rejection per ARINC specification 429
- Automatic transmitter data timing
- Self test mode
- Parity functions
- Low power
- Industrial & full military temperature ranges

**PIN CONFIGURATION (Top View)**

(See page 13 for additional pin configurations)
## PIN DESCRIPTION

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>FUNCTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>POWER</td>
<td>+5V ±5%</td>
</tr>
<tr>
<td>V+</td>
<td>POWER</td>
<td>+9.5V to +10.5V</td>
</tr>
<tr>
<td>V-</td>
<td>POWER</td>
<td>-9.5V to -10.5V</td>
</tr>
<tr>
<td>429DI1 (A)</td>
<td>INPUT</td>
<td>ARINC receiver 1 positive input</td>
</tr>
<tr>
<td>429DI1 (B)</td>
<td>INPUT</td>
<td>ARINC receiver 1 negative input</td>
</tr>
<tr>
<td>429DI2 (A)</td>
<td>INPUT</td>
<td>ARINC receiver 2 positive input</td>
</tr>
<tr>
<td>429DI2 (B)</td>
<td>INPUT</td>
<td>ARINC receiver 2 negative input</td>
</tr>
<tr>
<td>D/RT</td>
<td>OUTPUT</td>
<td>Receiver 1 data ready flag</td>
</tr>
<tr>
<td>D/R2</td>
<td>OUTPUT</td>
<td>Receiver 2 data ready flag</td>
</tr>
<tr>
<td>SEL</td>
<td>INPUT</td>
<td>Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2)</td>
</tr>
<tr>
<td>ENT</td>
<td>INPUT</td>
<td>Data Bus control, enables receiver 1 data to outputs</td>
</tr>
<tr>
<td>EN2</td>
<td>INPUT</td>
<td>Data Bus control, enables receiver 2 data to outputs if ENT is high</td>
</tr>
<tr>
<td>BD15</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD14</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD13</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD12</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD11</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD10</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD09</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD08</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD07</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD06</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>GND</td>
<td>POWER</td>
<td>0 V</td>
</tr>
<tr>
<td>BD05</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD04</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD03</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD02</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD01</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>BD00</td>
<td>I/O</td>
<td>Data Bus</td>
</tr>
<tr>
<td>TX/R</td>
<td>OUTPUT</td>
<td>Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty.</td>
</tr>
<tr>
<td>PLT</td>
<td>INPUT</td>
<td>Latch enable for byte 1 entered from data bus to transmitter FIFO.</td>
</tr>
<tr>
<td>PL2</td>
<td>INPUT</td>
<td>Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow PLT.</td>
</tr>
<tr>
<td>TXA(OUT)</td>
<td>OUTPUT</td>
<td>Line driver output - A side</td>
</tr>
<tr>
<td>TXB(OUT)</td>
<td>OUTPUT</td>
<td>Line driver output - B side</td>
</tr>
<tr>
<td>ENTX</td>
<td>INPUT</td>
<td>Enable Transmission</td>
</tr>
<tr>
<td>CWSTR</td>
<td>INPUT</td>
<td>Clock for control word register</td>
</tr>
<tr>
<td>CLK</td>
<td>INPUT</td>
<td>Master Clock input</td>
</tr>
<tr>
<td>TX CLK</td>
<td>OUTPUT</td>
<td>Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80.</td>
</tr>
<tr>
<td>MR</td>
<td>INPUT</td>
<td>Master Reset, active low</td>
</tr>
<tr>
<td>TEST</td>
<td>INPUT</td>
<td>Disable Transmitter output if high (pull-down)</td>
</tr>
</tbody>
</table>
FUNCTIONAL DESCRIPTION (cont.)

CONTROL WORD REGISTER

The HI-8599 contains 10 data flip flops whose D inputs are connected to the data bus and clocks connected to CWSTR. Each flip flop provides options to the user as follows:

<table>
<thead>
<tr>
<th>DATA BUS PIN</th>
<th>FUNCTION</th>
<th>CONTROL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BDO5</td>
<td>SELF TEST</td>
<td>0 = ENABLE</td>
<td>If enabled, the transmitter’s digital outputs are internally connected to the receiver logic inputs</td>
</tr>
<tr>
<td>BDO6</td>
<td>RECEIVER 1 DECODER</td>
<td>1 = ENABLE</td>
<td>If enabled, ARINC bits 9 and, 10 must match the next two control word bits</td>
</tr>
<tr>
<td>BDO7</td>
<td>-</td>
<td>-</td>
<td>If Receiver 1 Decoder is enabled, the ARINC bit 9 must match this bit</td>
</tr>
<tr>
<td>BDO8</td>
<td>-</td>
<td>-</td>
<td>If Receiver 1 Decoder is enabled, the ARINC bit 10 must match this bit</td>
</tr>
<tr>
<td>BDO9</td>
<td>RECEIVER 2 DECODER</td>
<td>1 = ENABLE</td>
<td>If enabled, ARINC bits 9 and 10 must match the next two control word bits</td>
</tr>
<tr>
<td>BD10</td>
<td>-</td>
<td>-</td>
<td>If Receiver 2 Decoder is enabled, then ARINC bit 9 must match this bit</td>
</tr>
<tr>
<td>BD11</td>
<td>-</td>
<td>-</td>
<td>If Receiver 2 Decoder is enabled, then ARINC bit 10 must match this bit</td>
</tr>
<tr>
<td>BD12</td>
<td>INVERT XMTR PARITY</td>
<td>1 = ENABLE</td>
<td>Logic 0 enables normal odd parity and Logic 1 enables even parity output in transmitter 32nd bit</td>
</tr>
<tr>
<td>BD13</td>
<td>XMTR DATA CLK SELECT</td>
<td>0 = +10</td>
<td>CLK is divided either by 10 or 80 to obtain XMTR data clock</td>
</tr>
<tr>
<td>BD14</td>
<td>RCVR DTA CLK SELECT</td>
<td>0 = +10</td>
<td>CLK is divided either by 10 or 80 to obtain RCVR data clock</td>
</tr>
</tbody>
</table>

ARINC 429 DATA FORMAT

The following table shows the bit positions in exchanging data with the receiver or the transmitter. ARINC bit 1 is the first bit transmitted or received.

<table>
<thead>
<tr>
<th>ARINC BIT</th>
<th>DATA BUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>BD 15</td>
</tr>
<tr>
<td>12</td>
<td>BD 14</td>
</tr>
<tr>
<td>11</td>
<td>BD 13</td>
</tr>
<tr>
<td>10</td>
<td>BD 12</td>
</tr>
<tr>
<td>9</td>
<td>BD 11</td>
</tr>
<tr>
<td>8</td>
<td>BD 10</td>
</tr>
<tr>
<td>7</td>
<td>BD 09</td>
</tr>
<tr>
<td>6</td>
<td>BD 08</td>
</tr>
<tr>
<td>5</td>
<td>BD 07</td>
</tr>
<tr>
<td>4</td>
<td>BD 06</td>
</tr>
<tr>
<td>3</td>
<td>BD 05</td>
</tr>
<tr>
<td>2</td>
<td>BD 04</td>
</tr>
<tr>
<td>1</td>
<td>BD 03</td>
</tr>
<tr>
<td>0</td>
<td>BD 02</td>
</tr>
<tr>
<td></td>
<td>BD 01</td>
</tr>
<tr>
<td></td>
<td>BD 00</td>
</tr>
</tbody>
</table>

THE RECEIVERS

ARINC BUS INTERFACE

Figure 1 shows the input circuit for each receiver. The ARINC 429 specification requires the following detection levels:

- **STATE**
  - ONE: +6.5 Volts to +13 Volts
  - NULL: +2.5 Volts to -2.5 Volts
  - ZERO: -6.5 Volts to -13 Volts

The HI-8599 guarantees recognition of these levels with a common mode Voltage with respect to GND less than ±4V for the worst case condition (4.75V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

---

**FIGURE 1. ARINC RECEIVER INPUT**
FUNCTIONAL DESCRIPTION (cont.)

RECEIVER LOGIC OPERATION

Figure 2 is a block diagram showing each receiver’s logic.

BIT TIMING

ARINC 429 specifies the following timing for received data:

<table>
<thead>
<tr>
<th></th>
<th>HIGH SPEED</th>
<th>LOW SPEED</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIT RATE</td>
<td>100K BPS ± 1%</td>
<td>12K-14.5K BPS</td>
</tr>
<tr>
<td>PULSE RISE TIME</td>
<td>1.5 ± 0.5 µsec</td>
<td>10 ± 5 µsec</td>
</tr>
<tr>
<td>PULSE FALL TIME</td>
<td>1.5 ± 0.5 µsec</td>
<td>10 ± 5 µsec</td>
</tr>
<tr>
<td>PULSE WIDTH</td>
<td>5 µsec ± 5%</td>
<td>34.5 - 41.7 µsec</td>
</tr>
</tbody>
</table>

The HI-8581 and HI-8589 accepts signals meeting these specifications and rejects signals outside these tolerances using the method described here:

1. The timing logic requires an accurate 1.0 MHz clock source. Less than 0.1% error is recommended.

2. The sampling shift registers are 10 bits long and must show three consecutive Ones, Zeros or Nulls to be considered valid data. To qualify data bits, One or Zero in the upper bits of the sampling shift register must be followed by Null in the lower bits within the data bit time. A word gap Null requires three consecutive Nulls in both the upper and lower bits of the sampling shift register. This guarantees the minimum pulse width.

3. Each data bit must follow its predecessor by not less than 8 samples and not more than 12 samples. In this manner the bit rate is checked. With exactly 1 MHz input clock frequency, the acceptable data bit rates are as follows:

<table>
<thead>
<tr>
<th></th>
<th>HIGH SPEED</th>
<th>LOW SPEED</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA BIT RATE MIN</td>
<td>83K BPS</td>
<td>10.4K BPS</td>
</tr>
<tr>
<td>DATA BIT RATE MAX</td>
<td>125K BPS</td>
<td>15.6K BPS</td>
</tr>
</tbody>
</table>

4. The Word Gap timer samples the Null shift register every 10 input clocks (80 for low speed) after the last data bit of a valid reception. If the Null is present, the Word Gap counter is incremented. A count of 3 enables the next reception.

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). If the receiver decoder is enabled and the 9th and 10th ARINC bits match the control word program bits or if the receiver decoder is disabled, then EOS clocks the data ready flag flip flop to a “1”, D/R1 or D/R2 (or both) will go low. The data flag for a receiver remains low until after both ARINC bytes from that receiver are retrieved. This is accomplished by first activating EN with SEL, the byte selector, low to retrieve the first byte and then activating EN with SEL high to retrieve the second byte. EN1 retrieves data from receiver 1 and EN2 retrieves data from receiver 2.

If another ARINC word is received and a new EOS occurs before the two bytes are retrieved, the data is overwritten by the new word.

---

**Figure 2. RECEIVER BLOCK DIAGRAM**
FUNCTIONAL DESCRIPTION (cont.)

RECEIVER PARITY

The Receiver Parity Check Enable bit (Control Register bit 4, CR4) controls how the 32nd bit of the received ARINC word is interpreted by the HI-3585 receiver.

When CR4 is set to a “0”, the 32nd bit is treated as data and transferred as received from the ARINC bus to the receive FIFO.

When CR4 is set to a “1”, the 32nd bit is treated as a parity error bit.

**Odd Parity Received**
The receiver expects the 32nd bit of the received word to indicate odd parity. If this is the case, the parity bit is reset to indicate correct parity was received and resulting word is written to the receive FIFO.

**Even Parity Received**
If the received word is even parity, the receiver sets the 32nd bit to a “1”, indicating a parity error. The resulting word is then written to the receive FIFO.

Therefore, when CR4 is set to “1”, the 32nd bit retrieved from the receiver FIFO will always be “0” when valid (odd parity) ARINC 429 words are received.

<table>
<thead>
<tr>
<th>CR4</th>
<th>ARINC BUS 32nd bit</th>
<th>FIFO 32nd bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>data</td>
<td>data</td>
</tr>
<tr>
<td>1</td>
<td>parity bit</td>
<td>Error Bit:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = odd parity</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = odd parity error (even parity)</td>
</tr>
</tbody>
</table>

DATA TRANSMISSION

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at either TXA(OUT) or TXB(OUT). The 31 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

<table>
<thead>
<tr>
<th></th>
<th>HIGH SPEED</th>
<th>LOW SPEED</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARINC DATA BIT TIME</td>
<td>10 Clocks</td>
<td>80 Clocks</td>
</tr>
<tr>
<td>DATA BIT TIME</td>
<td>5 Clocks</td>
<td>40 Clocks</td>
</tr>
<tr>
<td>NULL BIT TIME</td>
<td>5 Clocks</td>
<td>40 Clocks</td>
</tr>
<tr>
<td>WORD GAP TIME</td>
<td>40 Clocks</td>
<td>320 Clocks</td>
</tr>
</tbody>
</table>

The word counter detects when all loaded positions are transmitted and sets the transmitter ready flag, TX/R, high.

TRANSMITTER PARITY

The parity generator counts the ONES in the 31-bit word. If the BD12 control word bit is set low, the 32nd bit transmitted will make parity odd. If the control bit is high, the parity is even.

SELF TEST

If the BD05 control word bit is set low, the digital outputs of the transmitter are internally connected to the logic inputs of the receivers, bypassing the analog bus interface circuitry. Data to Receiver 1 is as transmitted and data to Receiver 2 is the complement. All data transmitted during self test is also present on the TXA(OUT) and TXB(OUT) line driver outputs. Taking TEST high forces TXA(OUT) and TXB(OUT) into the null state regardless of the state of BD05 control word bit.

SYSTEM OPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The received data may be overwritten if not retrieved within one ARINC word cycle.
2. The FIFO can store 8 words maximum and ignores attempts to load addition data if full.
3. Byte 1 of the transmitter data must be loaded first.
4. Either byte of the received data may be retrieved first. Both bytes must be retrieved to clear the data ready flag.
5. After ENTX, transmission enable, goes high it cannot go low until TX/R, transmitter ready flag, goes high. Otherwise, one ARINC word is lost during transmission.
FUNCTIONAL DESCRIPTION (cont.)

FIGURE 3. TRANSMITTER BLOCK DIAGRAM
The line driver in the HI-8599 is designed to directly drive the ARINC 429 bus. The two ARINC outputs (TXA(OUT) and TXB(OUT)) provide a differential voltage to produce a +10 volt One, a -10 volt Zero, and a 0 volt Null. Setting Control Register bit 13 to zero causes a slope of 1.5 $\mu$s on the ARINC outputs. A one in Control Register bit 13 causes a slope of 10 $\mu$s. Timing is set by on-chip resistor and capacitor and tested to be within ARINC requirements. No additional hardware is required to control the slope. The HI-8599 has 10 ohms in series with each line driver output, and is for applications where additional external series resistance is required, such as lightning protection.

**REPEATER OPERATION**

Repeater mode of operation allows a data word that has been received by the HI-8599 to be placed directly into its FIFO for transmission. Repeater operation is similar to normal receiver operation. In normal operation, either byte of a received data word may be read from the receiver latches first by use of SEL input. During repeater operation however, the lower byte of the data word must be read first. This is necessary because, as the data is being read, it is also being loaded into the FIFO and the transmitter FIFO is always loaded with the lower byte of the data word first. Signal flow for repeater operation is shown in the Timing Diagrams section.

The "-10" version of the HI-8599 product require a 10 Kohm resistor to be placed in series with each ARINC input without affecting the ARINC input thresholds. This option is especially useful in applications where external lightning protection is required.

Each ARINC input pin must be connected to the ARINC bus through a 10 Kohm resistor in order for the chip to properly detect the correct ARINC levels. The typical 10 volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 10 Kohm resistors, they are just below the standard 6.5 volt minimum ARINC data threshold and just above the 2.5 volt maximum ARINC null threshold.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

**POWER SUPPLY SEQUENCING**

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is $V+$ followed by $V_{cc}$, always ensuring that $V+$ is the most positive supply. The $V-$ supply is not critical and can be asserted at any time.
TIMING DIAGRAMS (cont.)

RECEIVER OPERATON

DATA READY FLAG D/R

BYTE SELECT SEL

ENABLE BYTE ON BUS EN

DATA BUS

TRANSMITTER OPERATION

DATA BUS

BYTE 1 VALID

BYTE 2 VALID

TRANSMITTING DATA

V_DIF (TXA(OUT) - TXB(OUT))

HI-8599

HOLT INTEGRATED CIRCUITS

8
### TIMING DIAGRAMS (cont.)

#### REPEATER OPERATION TIMING

- **429DI**
  - BIT 32

- **D/R**
  - t\(_{D/R}\)
  - t\(_{DIREN}\)
  - t\(_{EN}\)
  - t\(_{ENEN}\)
  - t\(_{EN}\)

- **EN**
  - t\(_{SELEN}\)
  - t\(_{ENSEL}\)

- **SEL**
  - DON'T CARE
  - t\(_{SELEN}\)
  - DON'T CARE

- **PL1**
  - t\(_{ENPL}\)
  - t\(_{PLEN}\)

- **PL2**
  - t\(_{ENPL}\)
  - t\(_{PLEN}\)

- **TX/R**
  - t\(_{TX/R}\)

- **ENTX**
  - t\(_{ENDAT}\)

- **TXA(OUT)**
  - BIT 1

- **TXB(OUT)**
  - BIT 32

- **END/R**

- **EN/REN**

- **EN**

- **NULL**
**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>Vcc</td>
<td>.................</td>
<td>-0.3V to +7V</td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td>V+</td>
<td>.................</td>
<td>+12.5V</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td>V-</td>
<td>.................</td>
<td>-12.5V</td>
<td>-13.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage at ARINC inputs</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VH</td>
<td>Common mode voltage less than ±4V</td>
<td>6.5</td>
<td>10.0</td>
</tr>
<tr>
<td></td>
<td>VI</td>
<td>less than ±4V with respect to GND</td>
<td>-2.5</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage at any other pin</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VH</td>
<td>DC Current Drain per pin</td>
<td>±10mA</td>
<td></td>
</tr>
</tbody>
</table>

| Storage Temperature Range: | Minimum | Typical | Maximum | °C |
|---------------------------|---------|---------|---------|
| -65°C to +150°C | -65°C | 0°C | +150°C |

<table>
<thead>
<tr>
<th>Soldering Temperature (Leads)</th>
<th>Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>280°C for 10 seconds</td>
<td>null respect to GND</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>2.5</td>
<td>0</td>
<td>V</td>
</tr>
</tbody>
</table>

**DC ELECTRICAL CHARACTERISTICS**

**Vcc = 5V ±5%, V+ = 10V , V- = -10V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARINC INPUTS</td>
<td>ONE</td>
<td>Differential Input Voltage: (429DI1(A) to 429DI1(B); 429DI2(A) to 429DI2(B))</td>
<td>VH</td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td>ZERO</td>
<td>To GND</td>
<td>-450</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td>NULL</td>
<td>To Vcc</td>
<td>2.5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Differential Input Resistance:</td>
<td>R</td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td></td>
<td>To GND</td>
<td>R</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>To Vcc</td>
<td>R</td>
<td>12</td>
<td>27</td>
</tr>
<tr>
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<td>Input Current:</td>
<td>I</td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td></td>
<td>Input Sink</td>
<td>I</td>
<td>-1.5</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>Input Source</td>
<td>I</td>
<td>50</td>
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<th>BI-DIRECTIONAL INPUTS</th>
<th>Symbol</th>
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<th>Limits</th>
<th>Unit</th>
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<tr>
<td>Input Voltage:</td>
<td>VH</td>
<td>Input Voltage LO</td>
<td>2.1</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>VL</td>
<td></td>
<td></td>
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<table>
<thead>
<tr>
<th>OTHER INPUTS</th>
<th>Symbol</th>
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<th>Limits</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Input Voltage:</td>
<td>VH</td>
<td>Input Voltage LO</td>
<td>2.7</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>VL</td>
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</table>

<table>
<thead>
<tr>
<th>Input Current:</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Sink</td>
<td>I</td>
<td></td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>
**DC ELECTRICAL CHARACTERISTICS (cont.)**

Vcc = 5V ±5%, V+ = 10V, V- = -10V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>LIMITS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ARINC OUTPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ARINC output voltage</td>
<td>VOOUT</td>
<td>no load and magnitude at pin</td>
<td>4.50</td>
<td>5.00</td>
</tr>
<tr>
<td>One or zero</td>
<td>VOUT</td>
<td></td>
<td>-0.25</td>
<td>0.25</td>
</tr>
<tr>
<td>Null</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ARINC output current</td>
<td>IOUT</td>
<td></td>
<td></td>
<td>80</td>
</tr>
<tr>
<td><strong>OTHER OUTPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage:</td>
<td>Logic &quot;1&quot; Output Voltage</td>
<td>VOH</td>
<td>IOL = -1.5mA</td>
<td>2.7</td>
</tr>
<tr>
<td>Logic &quot;0&quot; Output Voltage</td>
<td>VOL</td>
<td>IOH = 2.6mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Current:</td>
<td>Output Sink</td>
<td>IOL</td>
<td>VOUT = 0.4V</td>
<td>3.0</td>
</tr>
<tr>
<td>(Bi-directional Pins)</td>
<td>Output Source</td>
<td>IOH</td>
<td>VOUT = Vcc - 0.4V</td>
<td></td>
</tr>
<tr>
<td>Output Current:</td>
<td>Output Sink</td>
<td>IOL</td>
<td>VOUT = 0.4V</td>
<td>2.6</td>
</tr>
<tr>
<td>(All Other Outputs)</td>
<td>Output Source</td>
<td>IOH</td>
<td>VOUT = Vcc - 0.4V</td>
<td></td>
</tr>
<tr>
<td>Output Capacitance:</td>
<td>CO</td>
<td></td>
<td></td>
<td>15</td>
</tr>
</tbody>
</table>

**Operating Voltage Range**

| | VCC | 4.75 | 5.25 | V |
| | V+ | 9.5 | 10.5 | V |
| | V- | -9.5 | -10.5 | V |

**Operating Supply Current**

| | | | |
| | VCC | ICC1 | 20 | mA |
| | V+ | IDD1 | 16 | mA |
| | V- | IEE1 | 16 | mA |
## AC ELECTRICAL CHARACTERISTICS

\[ Vcc = 5V, V+ = 10V, V- = -10V, GND = 0V, TA = \text{Operating Temp. Range and } f \text{ clock} = 1MHz \pm 0.1\% \text{ with 60/40 duty cycle} \]

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CONTROL WORD TIMING</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width - \textit{CWSTR}</td>
<td>\textit{tCWSTR}</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Setup - DATA BUS Valid to \textit{CWSTR HIGH}</td>
<td>\textit{tCWSET}</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Hold - \textit{CWSTR HIGH} to DATA BUS Hi-Z</td>
<td>\textit{tCWHL}</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td><strong>RECEIVER TIMING</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay - Start ARINC 32nd Bit to \textit{D/R LOW}: High Speed</td>
<td>\textit{tdr}</td>
<td>16</td>
<td>(\mu)s</td>
</tr>
<tr>
<td></td>
<td>Low Speed</td>
<td>\textit{tdr}</td>
<td>128</td>
</tr>
<tr>
<td>Delay - \textit{D/R LOW} to \textit{EN LOW}</td>
<td>\textit{tdREN}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Delay - \textit{EN LOW} to \textit{D/R HIGH}</td>
<td>\textit{tENDR}</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>Setup - SEL to \textit{EN LOW}</td>
<td>\textit{tSELEN}</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Hold - SEL to \textit{EN HIGH}</td>
<td>\textit{tSENSEL}</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Delay - \textit{EN LOW} to DATA BUS Valid</td>
<td>\textit{tENDATA}</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Delay - \textit{EN HIGH} to DATA BUS Hi-Z</td>
<td>\textit{tDATAEN}</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Pulse Width - \textit{ENT} or \textit{ENZ}</td>
<td>\textit{tEN}</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Spacing - \textit{EN HIGH} to next \textit{EN LOW}</td>
<td>\textit{tENEN}</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td><strong>FIFO TIMING</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width - \textit{PL1} or \textit{PL2}</td>
<td>\textit{tPL}</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Setup - DATA BUS Valid to \textit{PE HIGH}</td>
<td>\textit{tDWSSET}</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Hold - \textit{PE HIGH} to DATA BUS Hi-Z</td>
<td>\textit{tDWHLD}</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Spacing - \textit{PL1} or \textit{PL2}</td>
<td>\textit{tPL12}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Delay - \textit{PL2 HIGH} to TX/R LOW</td>
<td>\textit{ttXR}</td>
<td>840</td>
<td>ns</td>
</tr>
<tr>
<td><strong>TRANSMISSION TIMING</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spacing - \textit{PL2 HIGH} to \textit{ENTX HIGH}</td>
<td>\textit{tPL2EN}</td>
<td>0</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>Delay - 32nd ARINC Bit to \textit{TX/R HIGH}</td>
<td>\textit{ttXR}</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Spacing - \textit{TX/R HIGH} to \textit{ENTX LOW}</td>
<td>\textit{tENTX/R}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td><strong>LINE DRIVER OUTPUT TIMING</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay - \textit{ENTX HIGH} to \textit{TXA(OUT)} or \textit{TXB(OUT)}: High Speed</td>
<td>\textit{tENDAT}</td>
<td>25</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>Delay - \textit{ENTX HIGH} to \textit{TXA(OUT)} or \textit{TXB(OUT)}: Low Speed</td>
<td>\textit{tENDAT}</td>
<td>200</td>
<td>(\mu)s</td>
</tr>
<tr>
<td>Line driver transition differential times:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(High Speed)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>high to low</td>
<td>\textit{tX}</td>
<td>1.0</td>
<td>1.5</td>
</tr>
<tr>
<td>low to high</td>
<td>\textit{tX}</td>
<td>1.0</td>
<td>1.5</td>
</tr>
<tr>
<td>(Low Speed)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>high to low</td>
<td>\textit{tX}</td>
<td>5.0</td>
<td>10</td>
</tr>
<tr>
<td>low to high</td>
<td>\textit{tX}</td>
<td>5.0</td>
<td>10</td>
</tr>
<tr>
<td><strong>REPEATER OPERATION TIMING</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Delay - \textit{EN LOW} to \textit{PE LOW}</td>
<td>\textit{tENPL}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Hold - \textit{PE HIGH} to \textit{EN HIGH}</td>
<td>\textit{tPLEN}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Delay - \textit{TX/R LOW} to \textit{ENTX HIGH}</td>
<td>\textit{ttXR}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td><strong>MASTER RESET PULSE WIDTH</strong></td>
<td>\textit{tMR}</td>
<td>400</td>
<td>ns</td>
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<tr>
<td><strong>ARINC DATA RATE AND BIT TIMING</strong></td>
<td></td>
<td></td>
<td>(\pm 1%)</td>
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</table>
HI-8599

ADDITIONAL HI-8599 PIN CONFIGURATIONS
(See page 1 for the 44-Pin Plastic Quad Flat Pack (PQFP) pin configuration)

HI-8599PJ
HI-8599PJT
44-Pin Plastic J-Lead PLCC

HI-8599CJ
HI-8599CJT
44-Pin J-Lead CERQUAD

ORDERING INFORMATION

HI - 8599 xx x x - xx

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>INPUT SERIES RESISTANCE</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>BUILT-IN</td>
</tr>
<tr>
<td>No dash number</td>
<td>35 Kohm</td>
</tr>
<tr>
<td>-10</td>
<td>25 Kohm</td>
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<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>LEAD FINISH</th>
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<tbody>
<tr>
<td>Blank</td>
<td>Tin / Lead (Sn / Pb) Solder</td>
</tr>
<tr>
<td>F</td>
<td>100% Matte Tin (Pb-free, RoHS compliant)</td>
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</table>

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMPERATURE RANGE</th>
<th>FLOW</th>
<th>BURN IN</th>
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</thead>
<tbody>
<tr>
<td>I</td>
<td>-40°C TO +85°C</td>
<td>I</td>
<td>No</td>
</tr>
<tr>
<td>T</td>
<td>-55°C TO +125°C</td>
<td>T</td>
<td>No</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CJ</td>
<td>44 PIN CERQUAD J LEAD (44U) not available Pb-free</td>
</tr>
<tr>
<td>PJ</td>
<td>44 PIN PLASTIC J LEAD PLCC (44J)</td>
</tr>
<tr>
<td>PQ</td>
<td>44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PQS)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>OUTPUT SERIES RESISTANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>8599</td>
<td>10 Ohms</td>
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</table>

HOLT INTEGRATED CIRCUITS
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<tr>
<th>P/N</th>
<th>Rev</th>
<th>Date</th>
<th>Description of Change</th>
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<tr>
<td>DS8599</td>
<td>C</td>
<td>06/29/12</td>
<td>Added Revision History Page. Updated PQFP package drawing. Clarified the description of receiver parity. Updated minimum Input Voltage HI for Other Inputs.</td>
</tr>
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HI-8599 PACKAGE DIMENSIONS

44-PIN PLASTIC PLCC

**Package Type:** 44J

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Pin No. 1 IDENT</td>
<td>.045 x 45°</td>
</tr>
<tr>
<td>Pin No. 1</td>
<td>.690 ±.005 (17.526 ±.127) SQ.</td>
</tr>
<tr>
<td>BSC</td>
<td>.653 ±.004 (16.586 ±.102) SQ.</td>
</tr>
<tr>
<td>See Detail A</td>
<td>.173 ±.008 (4.394 ±.203)</td>
</tr>
<tr>
<td>SQ.</td>
<td>.610 ±.020 (15.494 ±.508)</td>
</tr>
</tbody>
</table>

**BSC** = “Basic Spacing between Centers” is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN J-LEAD CERQUAD

**Package Type:** 44U

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Pin No. 1 IDENT</td>
<td>.688 ±.005 max (17.475 ±.127) SQ.</td>
</tr>
<tr>
<td>BSC</td>
<td>.650 ±.010 (16.510 ±.254) SQ.</td>
</tr>
<tr>
<td>Pin No. 1</td>
<td>.039 ±.005 (.990 ±.127)</td>
</tr>
<tr>
<td>BSC</td>
<td>.019 ±.002 (.483 ±.051)</td>
</tr>
<tr>
<td>R</td>
<td>.035 ±.010 (.889 ±.254)</td>
</tr>
<tr>
<td>SQ. max</td>
<td>.050 ±.007 (1.270 ±.178)</td>
</tr>
</tbody>
</table>

**BSC** = “Basic Spacing between Centers” is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)
44-PIN PLASTIC QUAD FLAT PACK (PQFP)

See Detail A

BSC = “Basic Spacing between Centers” is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)