HOLT INC.
INTEGRATED CIRCUITS

AN-550

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Hardware Design Considerations For MIL-STD-1553 Terminals

Introduction

This application note provides recommendations for hardware design for bus interface circuitry within MIL-STD-1553 terminals. This document describes interface of terminal logic to the transceiver, transceiver connection to the bus isolation transformer, and transformer interconnect to the MIL-STD-1553 bus. Methods are described to achieve proper terminal operation that complies with the MIL-STD-1553B standard.

Comprised of both digital and analog circuitry, terminal design includes several important factors to consider related to device selection and placement, circuit routing, grounding, and the use of decoupling capacitors. In addition, designers should be mindful of several physical factors affecting MIL-STD-1553 terminal performance; these factors are discussed.

Figure 1 shows typical terminal interconnect to a MIL-STD-1553 bus. The standard defines two types of bus coupling. **Direct-coupled terminals** are connected to the bus by a stub cable not more than 1 foot (30cm) long. Although the application should use the shortest cable that meets physical interconnect needs, **transformer-coupled terminals** may use a stub cable up to 20 ft (6m) long. Most

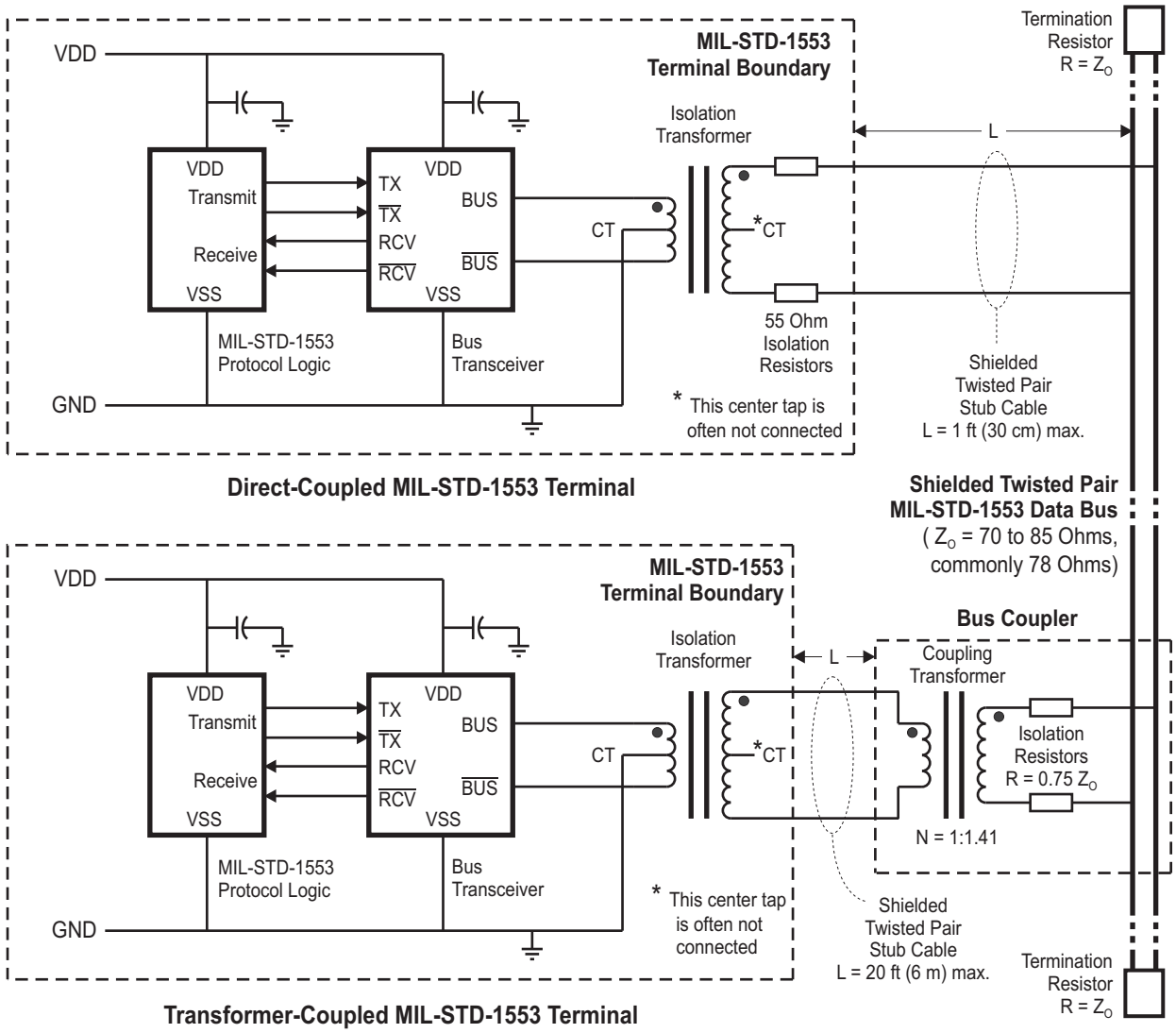


Figure 1. TRANSFORMER-COUPLED AND DIRECT-COUPLED TERMINALS

applications are transformer-coupled. Comprehensive information on direct- and transformer-coupled terminals is found in U. S. Dept. of Defense MIL-HDBK-1553A.

For clarity, Figure 1 shows just a single MIL-STD-1553 bus. Terminal isolation transformers and bus interconnect circuitry are repeated for the redundant bus. Figure 1 shows separate blocks for "Protocol Logic" and "Bus Transceiver" within the terminals. Sometimes the bus transceiver is contained within the protocol device; the Holt HI-6110 integrated message processor is an example.

Both configurations require an "isolation transformer" as part of the terminal hardware. The turns ratio for this transformer often differs for direct- and transformer-coupled operation, as well as for different MIL-STD-1553 transceiver part numbers and available power supply voltage. Dual-ratio isolation transformers are available from Holt to support either direct- or transformer-coupled applications. Hardware designs are often configurable within the terminal for either coupling type.

Direct-coupled (short stub) terminals use a pair of isolation resistors within the terminal itself. In contrast, transformer-coupled (long stub) terminals use an additional "coupling transformer" and a pair of series "isolation resistors" at the physical connection where the terminal's stub cable meets the MIL-STD-1553 bus cabling. In this case, the coupling transformer and resistors are generally inside an off-the-shelf "bus coupler" assembly.

Decoupling Capacitors

In any digital circuit, resistive and inductive conductor impedance causes voltage drops and resulting noise when high currents are conveyed from point to point on the board. Digital circuits clocked at high speed “gulp” current from the power supply at the clock frequency. Fast rise/fall times and distributed inductance contribute to common mode (L di/dt) noise on power supply wiring. Usual measures for noise control involve use of dedicated circuit board ground and power planes, and distributed use of decoupling capacitors to provide local, low impedance “charge reservoirs” to satisfy each integrated circuit's brief, increased demand for power supply current when clock edges occur.

Similarly, MIL-STD-1553 bus transceivers require local decoupling capacitors to satisfy current demand when transmitting. Transceivers work best when planar conductors are used for both power and ground. A monolithic ceramic capacitor (100nF) should be connected from each transceiver VDD pin to ground, using short, direct connections. Any terminal that transmits also requires a low ESR bulk storage capacitor for each transceiver VDD pin. A 22uF tantalum chip capacitor should be sufficient. If the application guarantees that concurrent transmission will not occur on both buses (a safe assumption in most MIL-STD-1553 designs) a single tantalum capacitor can serve the needs of both transmitters on a dual transceiver IC by bridging the device's VDD power pins together where the tantalum capacitor is connected. Each IC VDD pin should retain its own ceramic capacitor nearby.

Circuit Board Layout

As a precautionary measure to avoid crosstalk, avoid routing digital signals parallel to the MIL-STD-1553 bus analog board conductors, or on other layers in close proximity to the analog bus conductors. Crosstalk can couple digital noise onto the 1553 receiver circuit, reducing noise rejection performance.

The bus isolation transformer (and isolation resistors, if a direct-coupled terminal) should be placed close to the board's bus interface boundary, where the bus enters the circuit board. In addition, the transceiver should be located as physically close as possible to the isolation transformer. Close physical proximity reduces crosstalk and minimizes conductor voltage drops when transmitting, caused by wiring inductance. Because transceiver transmit currents can exceed 500mA, it is recommended to use minimum conductor trace widths of 0.04” (2.5mm) and use short, direct paths for transformer signal and center tap conductors.

Ground and Power Planes

When transmitting, the transformer center tap (on the transceiver IC side) conducts the large ground return currents, not the transceiver IC’s ground pin. Thus the ground conductor width for the center tap should at least match the analog drive conductor width, but ground plane can also be used for returning center tap currents to transceiver ground pin and power supply ground.

Bus side conductors from the transformer usually connect to 78 ohm twisted pair shielded cable. The decision of whether to isolate or make connections between the bus-side winding center tap, chassis ground and bus cable shielding should be made on a system basis after careful consideration of ESD, lightning and EMI concerns. In most cases, the bus side center tap is not connected for MIL-STD-1553 terminal applications.

While ground and power planes are recommended for the terminal's digital circuitry, it is important to avoid ground and power planes underneath the analog bus signal traces and under the bus isolation transformer. This is essential for meeting the MIL-STD-1553B requirement for input impedance. A ground or power plane under analog bus circuitry reduces input impedance at bus signaling frequencies.

MIL-STD-1553B requires 1000 ohm minimum input impedance for transformer-coupled terminals, and 2000 ohm minimum input impedance for direct-coupled

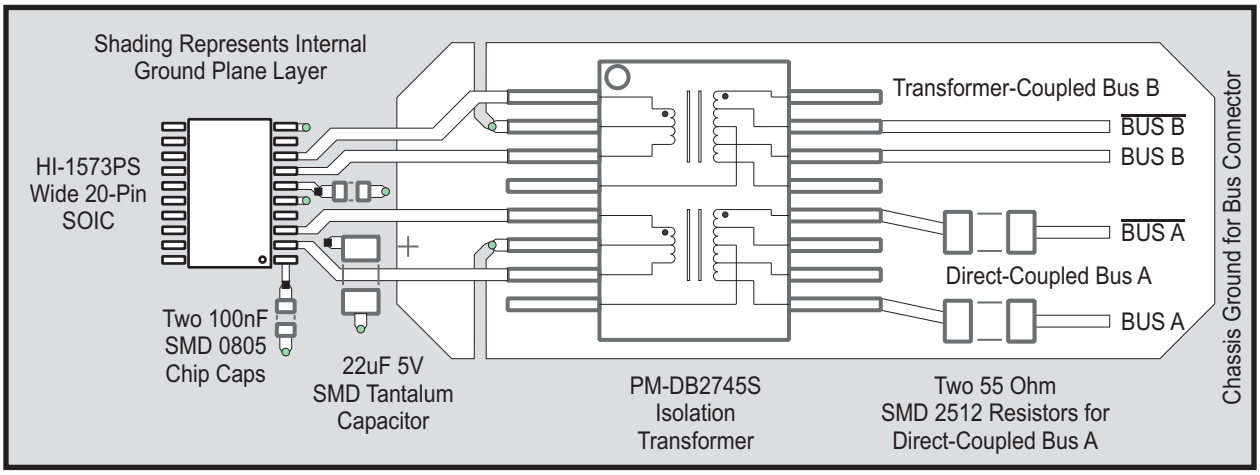
terminals, across the frequency range from 75 KHz to 1 MHz. The bus interface uses a pair of signal conductors on each side of the transformer. A plane under each analog bus conductor introduces capacitive coupling from the signal conductors to ground. This stray capacitance appears as a two capacitors in series, from one side of the bus to the other, (first signal conductor to ground, then ground to other signal conductor). This shunt capacitance reduces input impedance at the 1 MHz end of the tested frequency range. Avoiding ground and power planes underneath transceiver and transformer analog bus signal traces minimizes this effect.

Figures 2 and 3 show printed circuit board layouts for typical Holt MIL-STD-1553 devices, a HI-1573 transceiver in a 20-pin SOIC package, and a HI-6110 protocol device in the 52-pin PQFP package.

Isolation Transformer Selection

Transformer selection is another factor affecting input impedance. MIL-STD-1553B requires a minimum open circuit transformer input impedance of 3000 ohms, looking into the isolation transformer winding from the bus side, measured from 75 KHz to 1 MHz. The critical factors in achieving the 3000 ohm open circuit impedance is the distributed capacitance of the windings and the transformer primary inductance.

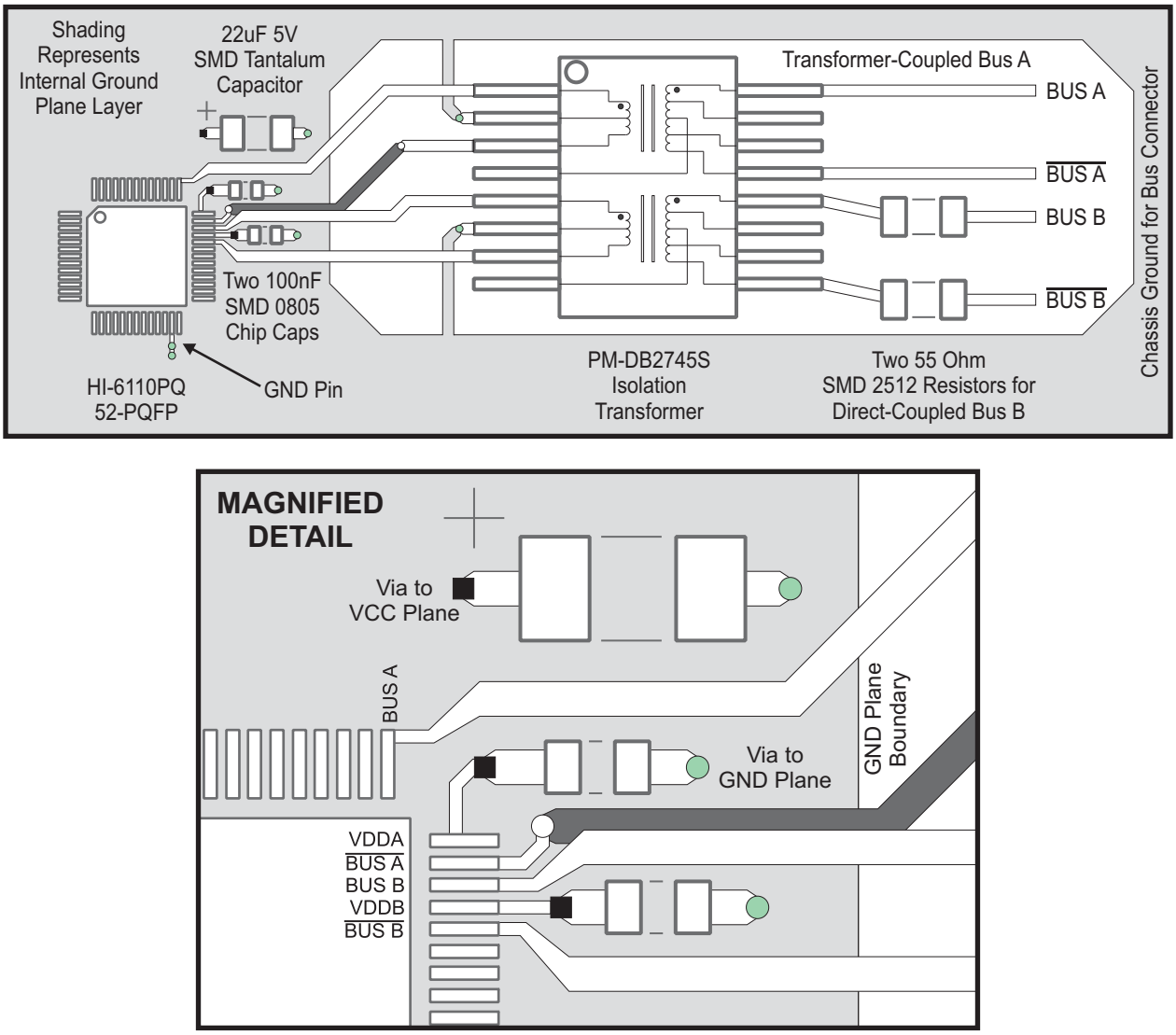
Manufacturers of MIL-STD-1533 transformers carefully balance design parameters to meet conflicting performance needs. For example, transformer inductance must be large enough to provide the minimum open circuit impedance at 75 KHz while the distributed capacitance should be small enough to maintain open circuit



Example Circuit Board Layout for Transceiver (e.g. HI-1573PS)

Explanatory Notes:
1. Component sizes are approximately to scale. Compromises were necessary in trying to portray a multilayer design in a single graphic. The layout assumes conventional 4-layer construction with internal Ground and Power planes and external signal routing layers on top and bottom.
2. The layout shows Bus A configured as direct coupled (having 55 Ohm isolation resistors) and Bus B configured as transformer-coupled. A conventional layout would probably not use mixed coupling modes. Notice that the HI-1573 uses the 2.50:1 transformer turns ratio for direct-coupled bus and 1.79:1 for transformer-coupled bus.
3. Bus connectors and pictured circuitry are placed close to board edge to minimize crosstalk.
4. No Ground plane or Power plane is poured under the transformer or analog bus signals to minimize shunt capacitance which affects terminal input impedance at high frequency. The light grey area represents the region where Ground and Power planes are present.
5. Circuit board “vias” make connections between layers.
6. All three surface mount capacitors have vias connecting both ends to their respective Ground and Power planes. Where space permits, 2 doubled-up vias on power and ground terminals (and high current signal conductors) provide a current path with lower inductance than a single via.

Figure 2. EXAMPLE CIRCUIT BOARD LAYOUT FOR TRANSCEIVER



Example Circuit Board Layout for HI-6110

Explanatory Notes:
1. Component sizes are approximately to scale. Compromises were necessary in trying to portray a multilayer design in a single graphic. The layout assumes conventional 4-layer construction with internal Ground and Power planes and external signal routing layers on top and bottom. The black trace segment should be routed on the bottom of the board.
2. The layout shows Bus A configured as transformer-coupled and Bus B configured as direct coupled (having 55 Ohm isolation resistors). A conventional layout would probably not use mixed coupling modes. Notice that the HI-6110 uses the same 2.50:1 transformer turns ratio for both coupling methods.
3. Bus connectors and pictured circuitry are placed close to board edge to minimize crosstalk.
4. No Ground plane or Power plane is poured under the transformer or analog bus signals to minimize shunt capacitance which affects terminal input impedance at high frequency. The light grey area represents the region where Ground and Power planes are present.
5. Circuit board “vias” make connections between layers.
6. All three surface mount capacitors have vias connecting both ends to their respective Ground and VCC planes. Where space permits, 2 doubled-up vias on power and ground terminals (and high current signal conductors) provide a current path with lower inductance than a single via.
7. Ideally, the 22uF bulk storage capacitor would be placed on the bottom, located closer to the two 100nF capacitors with (+) side connected to the VDD-Power vias for both 100nF capacitors.

Figure 3. EXAMPLE CIRCUIT BOARD LAYOUT FOR PROTOCOL DEVICE

impedance at 1 MHz. Inductance is easily increased by increasing the number of turns on the transformer, but this tends to increase distributed capacitance, degrading high frequency performance and causing waveform integrity and common mode rejection to suffer. Holt Integrated Circuits offers MIL-STD-1553 transformers optimized to work with its devices and there are other suitable transformers on the market. **Be sure to choose a transformer specifically optimized for use in MIL-STD-1553 terminals.** Naturally, the correct transformer turns ratio must be chosen for compatibility with the transceiver used.

Transmit-Induced "Tailoff" (Offset)

MIL-STD-1553B (4.5.2.1.1.4) has requirements for transmit signal "output symmetry." The title "output symmetry" results from the fact that lack of symmetry in the transmitter design can cause a temporary DC voltage to appear on the transmitter's bus stub, possibly impairing the terminal's ability to decode received commands for a period of microseconds after the transmitted command is completed.

The cited MIL-STD-1553B paragraph states that the voltage on the bus shall be less than ±250mV for the period beginning 2.5µs after the midbit zero-crossing of the last bit of a transmitted message (less than ±90mV for direct-coupled terminals). The offset voltage present on the stub at the end of a transmitted message is called "tailoff". Tailoff is typically an exponentially decaying DC voltage (time constant is approximately 25µs) resulting from waveform imbalance. Graphical examples of transmit-induced tailoff are seen in Figure 4.

The MIL-STD-1553 transceiver drives the transformer using a pair of differential outputs. These signals must be very closely balanced, with very little time skew between them. Properly encoded MIL-STD-1553 words have balanced signal waveforms. The positive area of the voltage waveform equals the negative area of the waveform.

Tailoff occurs after transmission and primarily affects the transmitting terminal. Seen at stubs for other receivers on the bus, tailoff voltage originating from another transformer-coupled terminal's transmission is attenuated to 1/4 amplitude by the bus network.

If the positive area of the transmitter output voltage waveform does not exactly equal the negative area of the waveform, residual stored charge will exist in the isolation transformer at the end of a transmission. Long messages will generally accumulate more stored charge than short messages. When transmission ends, this surplus charge drives a current into the transformer load impedance, causing tailoff voltage. Tailoff voltage decays exponentially; decay time varies depending on load resistance and inductance.

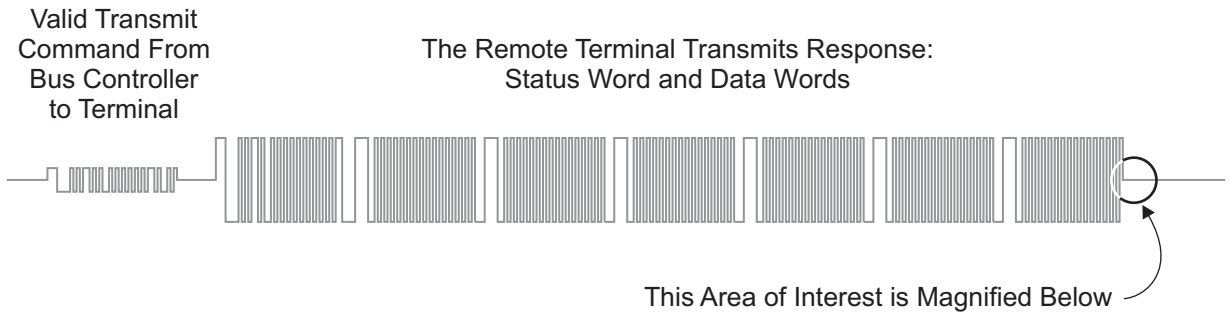
If the application uses a transceiver to interface a field programmable gate array (FPGA) or microprocessor to the MIL-STD-1553 bus, care must be taken to equalize the differential signal paths and propagation delays to minimize imbalance. The digital logic should be configured so that the differential drive signal pair uses high current buffer options to achieve fast, equal and concurrent edge transitions for transceiver drive signals.

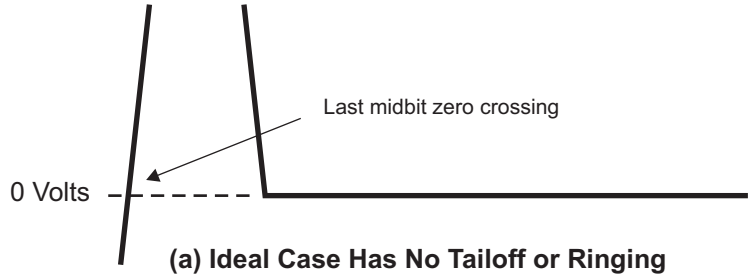
Even subtle imbalances lead to tailoff after transmission. Tailoff voltage is sensitive to data pattern; different transmitted data words produce different tailoff voltages. For example, a transmitted data word of all zeros, in the absence of any imbalance of any sort, produces a negative tailoff. This "default tailoff" is caused by the non-infinite load inductance and transmitter output impedance.

Other circuit imbalances add to this default tailoff to produce the observed tailoff voltage. For measuring tailoff, MIL-STD-1553B specifies that the maximum number of words allowable (usually 32) be transmitted. Sending the maximum number of words is assumed to be the worst case, although, due to the exponentially decaying nature of tailoff voltage, only the 10 to 12 most recently transmitted words make significant contributions to the tailoff. The standard also specifies that the test be done six times, with all the data words in each transmission set to 8000, 7FFF, 0000, FFFF, 5555, and AAAA (hexadecimal). One or the other of these data word patterns should be the worst case. Different transmitter-transceiver combinations display their worst tailoff with different data word patterns.

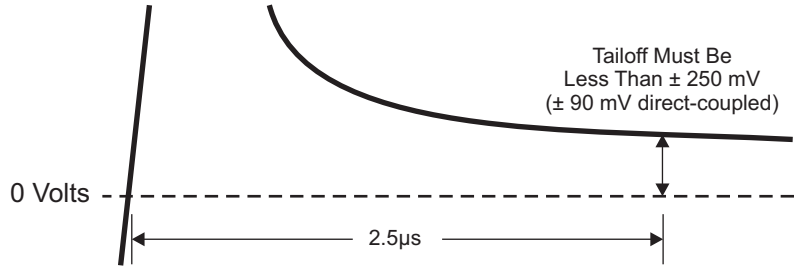
Design deficiencies that increase post-transmit tailoff include:

- Circuit layout imbalance caused by unequal differential signal conductors from transceiver to transformer (or from transformer to bus)
- Inadequate decoupling for the MIL-STD-1553 transceiver (or terminal logic driving the transceiver) that amplifies the effect of slight signal imbalance
- Unsuitable transformer in which the two halves of the driven winding have unbalanced leakage inductance or unbalanced parasitic capacitance.
- Using a transformer not optimized for MIL-STD-1553: At low temperature, transformer inductance decreases excessively, causing tailoff voltage
- The digital device driving the transceiver exhibits temperature dependent mismatch in high vs. low output drive characteristics, or rise/fall switching speed
- Using a socket for the transceiver or protocol device that adds ohmic resistance at the pin/socket interface, causing imbalance between bus drive signal conduction paths

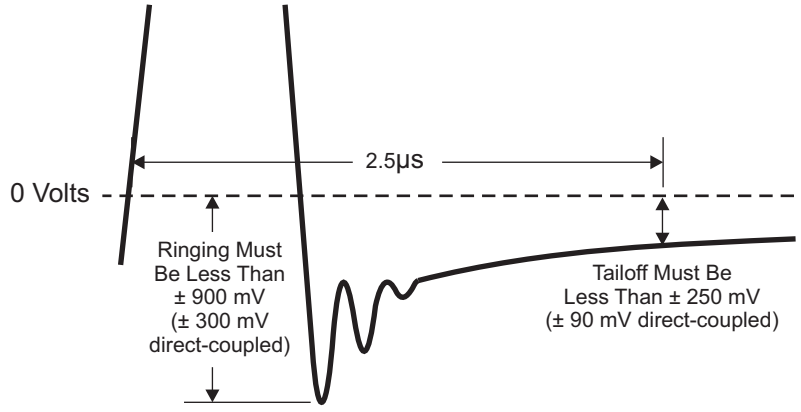




(a) Ideal Case Has No Tailoff or Ringing



(b) With Exponentially-Decaying Positive Tailoff



(c) With Ringing and Exponentially-Decaying Negative Tailoff

Figure 4. END OF TRANSMISSION (adapted from MIL-HDBK-1553A)

Intermessage Gap

Intermessage gap (4.3.3.7) is an input requirement, but compliance depends on the tailoff output characteristics. MIL-STD-1553B requires that a terminal must be able to respond to a message that is sent 4µs after the previous message. The worst-case condition for compliance occurs when the tailoff voltage after message transmission approaches the maximum allowed value of ±250mV (±90mV for direct-coupled stubs) at 2.5µs after the transmission, and the second message arrives after minimum 4µs intermessage gap.

The ±250mV tailoff requirement was designed to prevent the end of a transmission from interfering with the reception of the next message sent with the minimum intermessage gap of 4µs. With received signals just above receiver threshold and to the same terminal, this goal is not met. The gap test is typically done by sending two messages in close succession with a 4µs gap time.

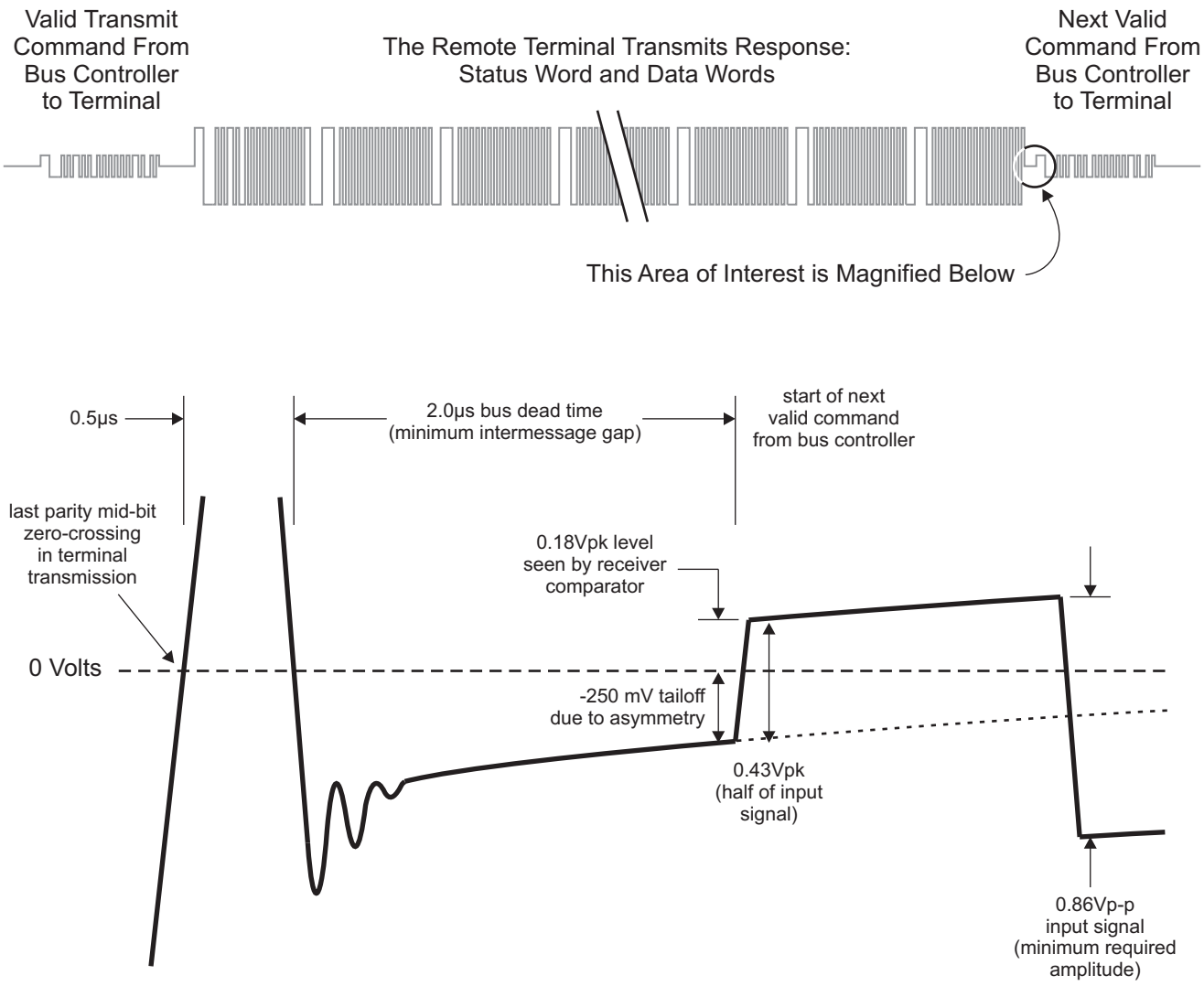
Figure 5 shows an example of minimum intermessage gap occurring between two messages on the input/output of a terminal for a transformer-coupled stub. The last half-bit of a transmission by the terminal is shown, followed in 4µs by the start of a command word from the bus controller. In this example, the terminal transmission has a tailoff voltage of negative 250mV after 2µs of bus “dead time.” This is the maximum tailoff level allowed by MIL-STD-1553B.

The received second message has a peak-to-peak amplitude of 860mVpp, the minimum required sensitivity required by MIL-STD-1553B. The receiver sees the first half-bit of the command word as a voltage level of 180mVpk, (860/2 - 250). The receiver would need to have a threshold voltage of 360mVpp to detect this half-bit properly, less than the minimum sensitivity required by MIL-STD-1553B. Decoding for the second message fails because the command sync is not properly decoded.

To determine the minimum amplitude of the second message so the gap test can pass, assume 860mVpp (430mV both positive and negative) for the receiver threshold. Add the tailoff of 250mV peak to these thresholds. This gives a minimum required voltage of 1.36Vpp for the second message. Note that the actual intermessage gap test for Remote Terminal Validation is performed with a receive signal amplitude of 2.1Vpp for transformer coupled devices (3.0Vpp for direct coupled).

Input Waveform Compatibility

The MIL-STD-1553 sections entitled “Input Waveform Compatibility” (4.5.2.1.2.1 and 4.5.2.2.2.1) state that a terminal must be able to correctly decode incoming signals that have up to ±150ns of error in any time interval between zero-crossings. Dealing with received waveform timing errors is primarily a function of the edge-detect and synchronization aspects of the MIL-STD-1553



This diagram shows stack-up of several worst-case conditions:

(1) asymmetry during terminal transmit causes the maximum tailoff level allowed by MIL-STD-1553B (±250 mV for transformer-coupled terminals)

(2) the next valid command to the transmitting terminal arrives after minimum intermessage gap of 4.0us, measured from mid-parity to mid-sync (equal to 2.0us bus dead time)

(3) signal amplitude for received command is equal to the minimum required receiver sensitivity (0.86Vpp)

The combination of conditions means the peak signal amplitude at the start of the following command, as seen by the receiver, is just 0.18Vpk. The minimum receiver threshold would have to be less than 2x this value, 0.36Vpp,to successfully detect the command sync. This is 0.5 Volt less than the minimum required receiver sensitivity, 0.86Vpp.

Figure 5. TAILOFF & MINIMUM INTERMESSAGE GAP (from MIL-HDBK-1553A)

Manchester II decoder. The role of the analog front end in the transceiver is to remove high frequency distortion and to add as little error as possible to the input waveform.

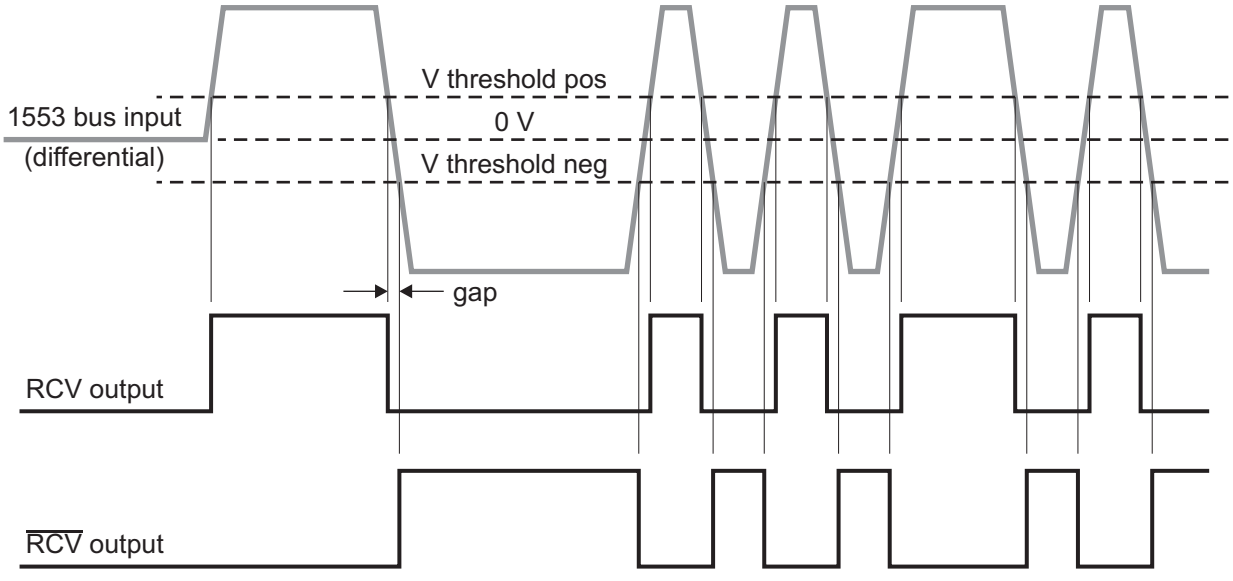
The analog bus receiver contains two voltage comparators that provide a pair of digital outputs to the decoder. One comparator has a negative threshold and thus detects negative excursions of the input signal from the bus, and the other has a positive threshold and detects positive bus excursions. MIL-STD-1553B requires bus waveform rise times and fall times to be 100 to 300ns, so transitions in the two comparator outputs occur at different times from the actual zero-crossing, One comparator switches a little earlier than the zero-crossing and the other switches a little later. The actual zero-crossing occurs between these two times. Ideally the zero-crossing will have happened halfway between the transitions of the two comparators, but unbalanced comparator thresholds modify this. If the decoder assumes that the comparator thresholds are balanced, this can introduce additional zero-crossing error into the signal seen by the decoder.

Figure 6 shows this graphically. The output of the positive comparator is RCV. The negative comparator output is $\overline{\text{RCV}}$. Vthreshold_pos is the threshold for the positive comparator and Vthreshold_neg is the threshold for the negative comparator. Below, the RCV output pulse is narrower than the corresponding positive excursion of the 1553 bus signal, and the $\overline{\text{RCV}}$ output pulse is wider for the same positive input excursion. Correspondingly, the RCV output pulse is wider and the $\overline{\text{RCV}}$ pulse is narrower than the negative excursion occurring in the 1553 bus signal.

MIL-STD-1553B states that transformer-coupled terminals shall respond to input signals of 0.86 to 14 Vpp and shall not respond to signals less than 0.2 Vpp. (For direct-coupled terminals, the levels are 1.2 to 20 Vpp and less than 0.28 Vpp.) Stated differently, the input threshold of the terminal, which is the voltage at which it detects an input signal, must be less than 0.86 Vpp and greater than 0.20 Vpp. (For direct-coupled, the levels are less than 1.2 and greater than 0.28 Vpp.) Restated yet again, the positive and negative input thresholds must each be less than 0.43 Vpk and greater than 0.1 Vpk (0.60 Vpk and 0.14 Vpk) if the positive and negative comparator thresholds are balanced. This represents the ideal performance for the analog front end in the MIL-STD-1553 bus receiver.

To meet these input requirements, it is essential to use an isolation transformer with the same turns ratio that was assumed when the MIL-STD-1553 transceiver was designed. The well-intentioned goal of increasing transmit amplitude by substituting a transformer with higher turns ratio means all the critical receiver thresholds will be wrong, causing impairment in receive performance.

The digital decoder also plays a role in determining the effective threshold of the terminal. As input amplitude is lowered, zero-crossing error can be introduced into the signal due to the nonzero rise and fall times of the input



The 100 to 300ns risetime / falltime requirement for MIL-STD-1553 signal transmission causes “gaps” between signal transitions at receive comparator outputs RCV and $\overline{\text{RCV}}$. The decoder must estimate actual the zero-crossing times occurring during the gaps between receiver output transitions. The gaps become wider (and difference in comparator output pulsewidth becomes more pronounced) as receive signal amplitude decreases, approaching the minimum peak-to-peak signal level that the receiver accepts.

Figure 6. RECEIVER WAVEFORM DECODING

signal, as discussed above. As the voltage of the input signal falls toward the receiver's threshold value, the signal is below the threshold for a greater part of each bit time. Thus there will be a greater difference in the transition times of the receiver outputs from the actual zero-crossings.

For applications where a transceiver interfaces a gate array, microprocessor or other digital logic to the MIL-STD-1553 bus, the logic designer must realize that the decoder's method of measuring its two inputs to estimate actual zero-crossing times determines its sensitivity to receiver output signal changes caused by amplitude variance. A decoder that poorly estimates actual zero-crossing times could reject a MIL-STD-1553 word because of zero-crossing errors, even though the receiver detected the word properly (i.e., was above receiver input threshold). The decoder usually attempts to choose a time halfway between the transitions of its inputs. Some methods are more successful than others at detecting the actual zero-crossing times. Any method attempting to use a single receiver output is doomed from the start. About all that can be said here is that the terminal design must be evaluated as a whole, not as separate transceiver and decoder.

Remote Terminal Validation Test for Zero-Crossing Distortion

To this point, discussion has focused on receiver signal output changes resulting from amplitude variation and threshold imbalance, while the received waveforms are assumed to have ideal zero-cross timing. In the real MIL-STD-1553 bus environment, actual zero-cross error appears on received bus signals as a result of signal reflections. As shown in Figure 7, reflected signals from downstream stubs cause shifts in zero-cross timing.

The decoder design must be tolerant of actual zero-cross distortion in the received signal. The following test defines the added requirement for zero-cross distortion. Using test input signal amplitude of 2.1Vpp for transformer coupled terminals (3.0Vpp for direct coupled) and all rise and fall times equal to 200 ±20ns, the terminal must tolerate any single zero-crossing within the received message shifted by ±150ns. Each zero-crossing in the message is individually tested with +150ns shift and separately with –150ns shift. No decoding error should occur in this test. All zero-cross distortion patterns are repeatedly tested.

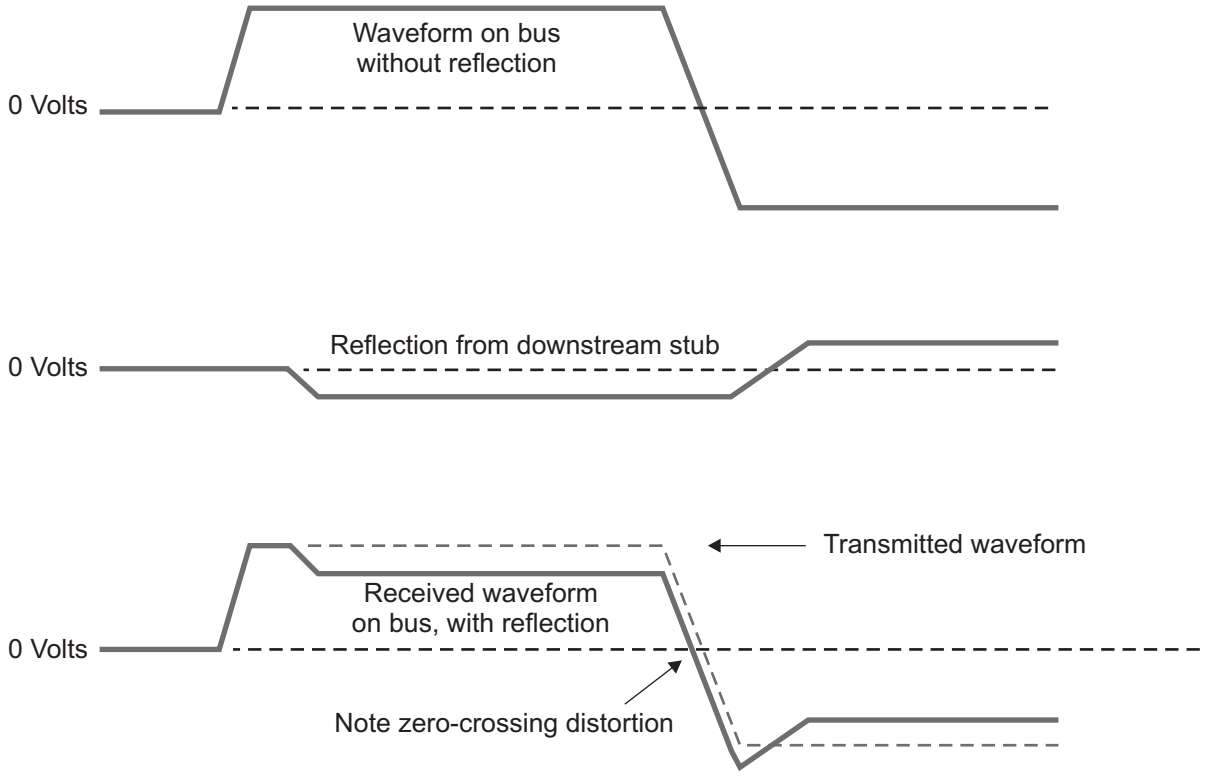


Figure 7. STUB REFLECTIONS CAUSE ZERO-CROSSING DISTORTION

Power Dissipation in 3.3V Devices

Users of Holt's 3.3V HI-1573 transceiver sometimes question an apparent discrepancy in the "DC Electrical Characteristics" for the device data sheet. Maximum power supply current IDD is specified at 500mA, when one bus is continuously transmitting. Thus 1.65W is drawn from the power supply (3.3V x 0.5A). However the HI-1573 data sheet says device power dissipation under this test condition is just 0.3W typical, 0.5W maximum.

The simple explanation is that most of the power is being dissipated in the load driven by the transceiver: the distributed bus impedance and bus terminating resistors. This is easily demonstrated on the test bench by replacing the MIL-STD-1553 bus with a load resistor. For a transformer-coupled terminal, a 78 ohm resistor is connected across the bus side of the terminal's isolation transformer. To achieve maximum power, the terminal hardware driving the HI-1573 is configured to continuously transmit Manchester-encoded MIL-STD-1553 words. If the test is run for more than a few seconds, it quickly becomes apparent that the 78 ohm resistor gets hot, and should be sized for 1.5W dissipation! Yet the HI-1573 transceiver is just warm.

The Holt HI-1573 transceiver is the most efficient in the industry, driving its load, the transformer winding, within 0.1V of the supply rail. It is far more efficient than 5V transceivers fabricated using older processes. Power transfer efficiency is a key feature of the HI-1573, making it an attractive part for new designs. This benefit also applies to the 3.3V HI-6110 protocol device.

In Conclusion

Awareness of the presented design constraints and recommendations should improve the designer's first-time results for MIL-STD-1553 terminal design.

REVISION HISTORY

Revision	Date	Page	Description of Change
AN-550, Rev. New	08/08/08	All	Initial release.